

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
BUR920010167US1

In Re Application Of: Aday, et al.

Serial No.
09/683,733Filing Date
02/07/02

Examiner

Group Art Unit

Title: **CUSTOM PRICING SYSTEM AND METHOD****RECEIVED**

Address to:

Assistant Commissioner for Patents
Washington, D.C. 20231

MAR 08 2002

Technology Center 2100**37 CFR 1.97(b)**

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:
- ☐ the statement specified in 37 CFR 1.97(e);
- OR**
- ☐ the fee set forth in 37 CFR 1.17(p).

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FEB 25 2002

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Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of _____ is attached.
- ☒ The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No.09-0456 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____
- ☐ Credit any overpayment.
- ☒ Charge any additional fee required.

Certificate of Transmission by Facsimile*

I certify that this document and authorization to charge deposit account is being facsimile transmitted to the United States Patent and Trademark Office (Fax. No. _____) on _____

(Date)

Signature

Typed or Printed Name of Person Signing Certificate

Certificate of Mailing by First Class Mail

I certify that this document and fee is being deposited on 02/12/02 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Pat Guillemette

Signature of Person Mailing Correspondence

Pat Guillemette

Typed or Printed Name of Person Mailing Certificate

*This certificate may only be used if paying by deposit account.

Richard M. Kotulak

Signature

Registration No. 27,712

International Business Machines Corporation

Intellectual Property Law - Mail 972E

1000 River Street

Essex Junction, VT 05452

Dated: 2/11/02

CC:

ET693515872US

IBM Docket #:BUR920010167US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Aday et al.

: Date: January 4, 2002

Serial Number: Concurrent

: Group Art Unit:

Filed: Concurrent

: Examiner:

Title: Custom Pricing System and Method

: IBM CORPORATION

Intellectual Property Law

: 1000 River Street, 972E

Essex Junction, Vermont 05452

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INFORMATION DISCLOSURE STATEMENT (IDS) UNDER 37 CFR 1.97

Commissioner For Patents

Washington, D. C. 20231

Dear Sir:

The attached Form PTO-1449, and any attached foreign patent office search report, provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:

X 37 CFR 1.97(b) - No Fee.

____ 37 CFR 1.97(c) - No Fee. Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application. This communication is dated _____, which is not more than 3 months prior to the mailing of this statement.

____ 37 CFR 1.97(c) - Fee.

____ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge payments of any associated fees required under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. 09-0456.

Respectfully submitted,

By:



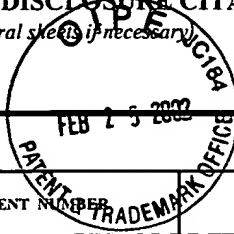
John W. LaBatt

Registration No. 48,301

Telephone No.: (518) 449-0044

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)



Docket Number (Optional)

BUR920010167US1

Application Number

09/683,733

Applicant(s)

Aday et al.

Filing Date

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Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US20010023418A1	09/2001	Suzuki et al.			
		US 6,249,776 B1	06/2001	Bajuk et al.			
		5,960,417	09/1999	Pan et al.			

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		P. K. Nag, W. Maly, and H. J. Jacobs, "Simulation of Yield/Cost Learning Curves with Y4," IEEE Transactions on Semiconductor Manufacturing, vol. 10, no. 2, pp. 256 - 266, May 1997.
		R. Ross, J. Bailey, N. Atchison, and M. Effron, "A Comprehensive Sequential Yield Analysis Methodology and the Financial Payback for Higher Yields," 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 80-86, 1999.

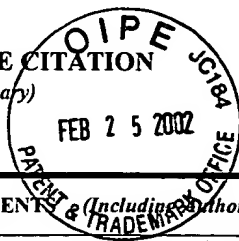
EXAMINER

DATE CONSIDERED

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(Use several sheets if necessary)



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INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

C. A. Moritz, D. Yeung, and A. Agarwal, "SimpleFit: A Framework for Analyzing Design Trade-Offs in Raw Architectures," IEEE Transactions on Parallel and Distributed Systems, vol. 12, no. 7, pp. 730-742, July 2001

G. A. Allan and A. J. Walton, "Fast Yield Prediction for Accurate Costing of ICs," 1996 Innovative Systems in Silicon Conference, Session 8: Yield & Testing, pp. 279-287, 1996.

nTool Solutions, <http://www.ntool.com/ntool/Solutions/Cps/Ndiesizer/Ndiesizer.html>, printed October 8, 2001.

"UMC UNVEILS CHIPSIZER: Online Tool Estimates Die Size and Silicon Cost," <http://www.umc.com/english/news/20001030.asp>, October 30, 2000.

"UMC Chipsizer" <http://eproject.umc.com/dse/>, printed October 8, 2001.

D. N. Maynard, R. J. Rosner, M. L. Kerbaugh, R. A. Hamilton, J. R. Bentlage, and C. A. Boye, "Wafer Line Productivity Optimization in a Multi-Technology Multi-Part-Number Fabricator," 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 34-42, 1998.

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